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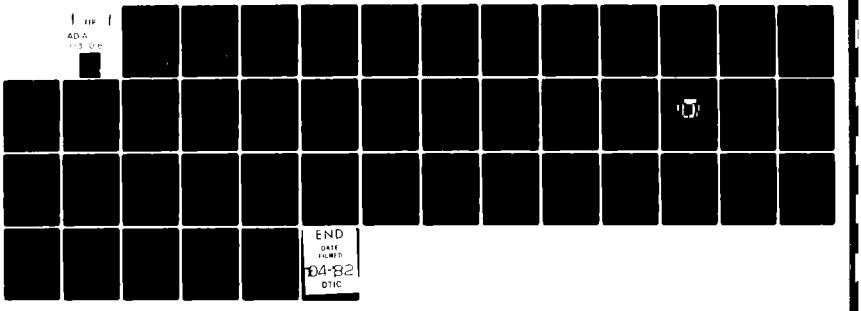

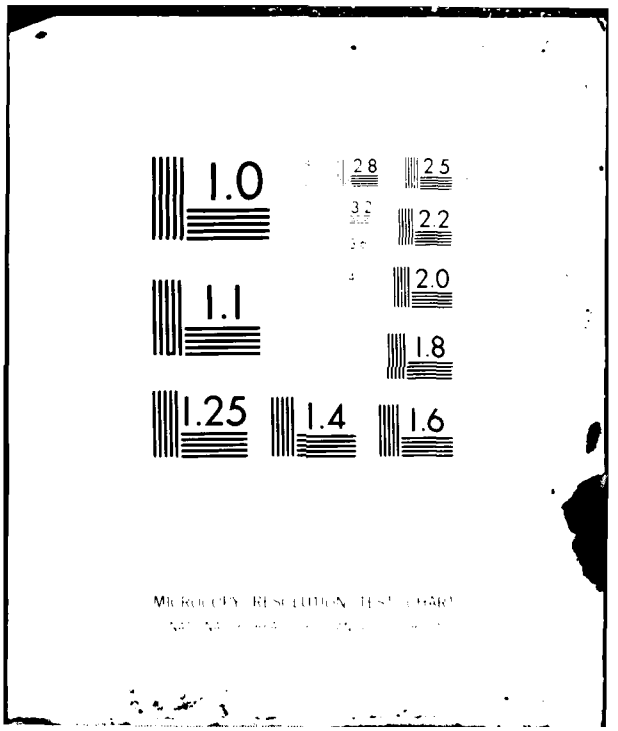
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MAGNETIC BUBBLE MEMORIES FOR DATA COLLECTION IN SOUNDING ROCKETS

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A survey was made to determine the feasibility of using magnetic bubble memories for data storage on board sounding rockets. The advantages and limitations of bubble memories are discussed along with factors influencing their use in sounding rockets. An Intel Magnetics 7110 Bubble Memory was selected as the most likely candidate for sounding rocket applications, and a system concept based on the 7110 is described.

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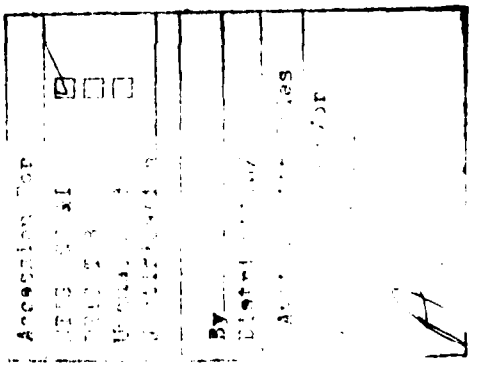
SUMMARY

This study was performed for the Air Force Geophysics Laboratory to determine the feasibility of using magnetic bubble memories for data storage on sounding rockets. A brief description of the principles and operating characteristics of bubble memories is presented. A survey of the availability of bubble memories for potential use in sounding rockets was conducted, and the Intel magnetics 7110 Bubble Memory was chosen as the most likely candidate for near-term sounding rocket applications. A discussion of the Intel Magnetics 7110 System, factors peculiar to the application of bubble memories in sounding rockets, and potential future developments of bubble memories are presented. The Intel 7110 is compared with a SETS-1 Digital Tape Recorder for sounding rocket applications with the result that the bubble memory has less storage capacity than the digital recorder (on a one-for-one basis), but bubbles are much more suitable for the physical environment imposed by sounding rockets. The study concludes that compactness, ruggedness, reliability and non-volatility are the major advantages of bubble memories for use in sounding rockets. However, considerable support circuitry is required for optimal use of bubble memories. And, although bubble memories with four megabit and higher storage capability are promised in the near future, the storage capacity of devices currently available is limited to one megabit. Considering these advantages and limitations, bubble memories are feasible for certain specific data storage applications on board sounding rockets.



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Magnetic Bubble Memories for Data Collection in Sounding Rockets

1. INTRODUCTION

After 10 years as a laboratory curiosity, magnetic bubble memory is now a matured commercial product. Non-volatility, reliability, compactness, and ruggedness make bubble memories a unique member of the storage hierarchy. This report will review magnetic bubble memories and discuss their potential applications in the sounding rocket program.

The sounding rocket program uses various methods of gathering scientific and other data. The bulk of this data is received via radio telemetry links and permanently stored on magnetic tape. With the advent of more sophisticated instruments and faster electronics as well as larger sounding rockets, the quantity of data to be stored during a rocket flight has increased significantly. With the expanding data requirements in the sounding rocket program and associated crowding of the R.F. spectrum, on board mass storage systems may become an attractive alternative for some applications. However, the mass storage system must be nonvolatile, low cost, fairly fast, reliable, compact, able to survive harsh environments, free of mechanical inertia, and have low power consumption.

The magnetic bubble memory appears to satisfy all these requirements to some degree. This investigation is to determine to what degree the bubble memory devices meet the above requirements and to what extent bubble memory systems might be utilized in the sounding rocket program.

2. BUBBLE MEMORY DESCRIPTION

The original concept of bubble memories was presented by Bell Laboratories in the late 1960s. Since that time, many companies have been actively pursuing the development of bubble memory devices.

Magnetic bubble memory chips are built by depositing a thin garnet film containing iron onto a non-magnetic garnet substrate. The atoms of iron combine with atoms of other elements in the film to behave like small magnets. The bonding forces within the garnet crystals orient these atoms parallel to their closest neighboring atoms. Magnetic domains form in the garnet film where groups of atoms align themselves in the same direction. These magnetic domains tend to form snake-like patterns of equal areas. Magnetic fields caused by the domains tend to line up perpendicular to the plane of the film.

By applying an external magnetic field perpendicular to the film, the domains having the same polarity as the field expand. Domains magnetized with the opposite polarity shrink. As the external field strength increases, the domains opposing the field shrink until they become small cylinders embedded in a background of opposite polarity (Figure 1).[1] If the field increases still further, the bubbles finally collapse. These bubbles are stable over a range of magnetic biases and can be made to move in the plane of the film with extremely small expenditures of energy.[2]

The practical application of this phenomenon is that these tiny magnetic "bubbles" can be used to represent digital data. The presence of a bubble represents a logic "1" and the absence of a bubble represents a "0". With diameters on the order of 1 to 5 micro-meters, these bubbles are so small that extremely tiny chips can hold thousands of bubbles.

Once magnetic bubbles have formed, a constant magnetic field maintains the bubbles.[2] Therefore, by placing a simple magnet next to a bubble memory chip, the data represented by the bubbles can be maintained without any applied power.

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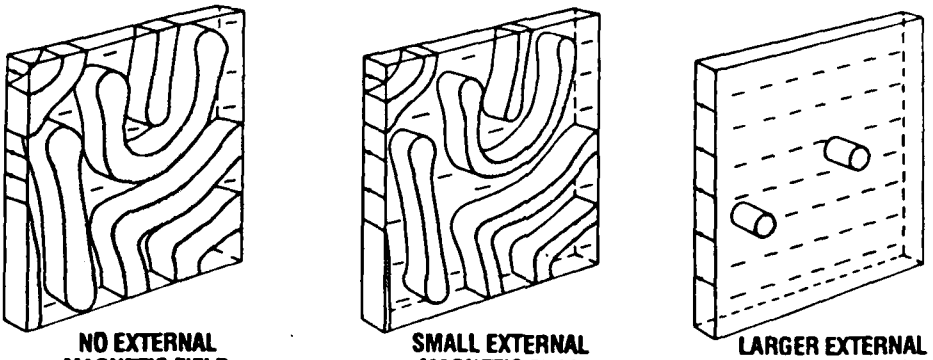
[1] Appendix H, Texas Instruments TBB5005/10 User's Manual

[2] Don Harmon, "Test Strategies Find Faults in User's Bubble Memories", Electronics, June 1, 1981, Page 145



EXTERNAL MAGNETIC FIELD SHRINKS RANDOM
SERPENTINE DOMAINS OF MAGNETICALLY NEUTRAL
CRYSTAL TO CYLINDRICAL FORM.

Figure 1. Magnetic Domain Shrinkage

When a thin film of magnetic garnet lies perpendicular to a magnetic field, tiny cylindrical portions of the material surface become magnetized.[1] Changing the direction of a second magnetic field that is parallel with the film moves the cylinders around the film surface. Rows of soft magnetic nickel-iron material (Permalloy) deposited on the top of the garnet film provide specific paths for bubbles. These magnetic areas are usually shaped like asymmetric chevrons. These Permalloy patterns act as small electromagnets whose polarity is induced and controlled by an external rotating field. Although other shapes may be used, asymmetric chevrons are more tolerant of manufacturing processes.[1] Moreover, asymmetric chevrons do not require geometrical features as small as other types largely because these chevrons are optimized for bubble propagation in only one direction. The bubbles are magnetic dipoles and therefore interact strongly, thus the chevrons must keep the bubbles separated by at least four bubble diameters.[2] The bubble diameter is a function of the garnet film composition and the applied bias field.[1]

The rotating magnetic field on bubble chips is provided by wrapping the entire chip with two mutually perpendicular wire coils. The coils are driven by triangular current waveforms 90-degrees out of phase with each other. This field moves bubbles around on the chip by sequentially magnetizing the chevrons. The bubbles cling to the magnetized chevrons and move under the chevron patterns as the field rotates (Figure 2).[1] The bubble movement does not entail moving solid matter since only magnetic field domains move through the crystal; therefore bubbles can move rapidly through the chip.

In order to write digital information onto the chip, a device is needed to generate bubbles; this is called a generate gate. Bubbles are generated by magnetic fields produced from microscopic hairpin-shaped aluminum loops fabricated on the surface of the garnet film. A pulse of electrical current through the loop produces a magnetic field on the film under the loop. This field opposes the field of the permanent magnets and creates a new magnetic bubble. Once a bubble is created, it is shifted around on the chip to a specific area for storage.

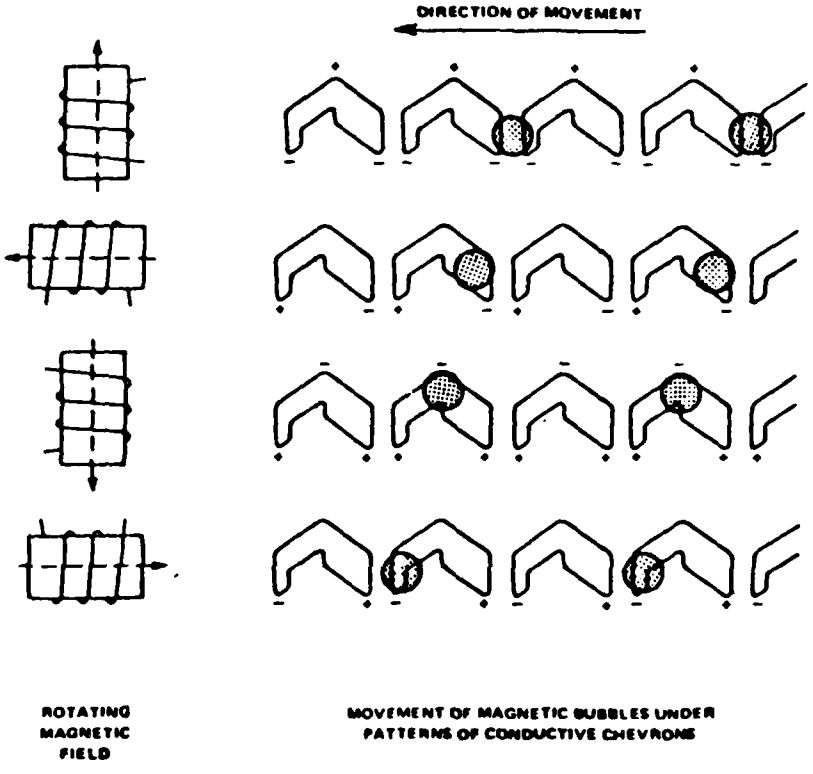


Figure 2. Bubble Movement Under Chevron Patterns

In order to read the information out of the chip a device is needed to detect the presence or lack of a bubble; this is called a detector gate. Once the rotating field has properly positioned the bubbles, the detector can sense the bubble's magnetic flux and convert it to data bit information. The bubble to be read moves under a small Permalloy structure connected to an aluminum lead. This structure, called a replicate gate, stretches and splits each bubble into two bubbles the same size as the original. One of these bubbles continues in the normal path (thus retaining the original data) while the other is steered toward a bubble detector. The bubble to be read then travels under several rows of symmetrical chevrons which stretch the bubble to a length that is several hundred times its normal diameter, and increases its stray flux by several orders of magnitude. The elongated bubble then passes under another Permalloy structure whose electrical resistance changes with changes in magnetic field strength. An elongated bubble passing under the detector area lowers the detector's electrical resistance. Thus the detector's electrical current increases when a bubble passes, and this increase is sensed by an external amplifier.

Before new data can be entered into a particular page position, the old data must be removed by doing a destructive read operation. This is the same as an ordinary read operation except that the bubbles are annihilated by transferring the bubble to the detector track without replication.

The easiest way to build a bubble memory is to build a device similar to a conventional shift register where an entered bubble moves through the long string of chevrons and is read out after a certain number of clock periods. However, a continuous shift register has two major drawbacks. First, the access time is very high because the bubbles must travel through the entire chip before reappearing to be read.

Second, in order for the bubbles to travel through the entire chip, the chip must be defect free. A single chevron defect ruins the entire chip. Defects come from various sources such as impurities in the garnet surface, irregularities in the garnet surface, or flaws in the photolithographic processing.[1]

One bubble memory scheme that allows for some flaws is the major-minor loop architecture. This architecture also provides a much faster access time and is the method most commonly used among manufacturers. In the major-minor loop architecture a large number of minor loops are placed perpendicular to the now shorter major loop.[3] These minor loops are placed so that they can transfer bubbles to and from the major loop. Thus a string of data placed into the major loop can be transferred to the first position in the minor loops simultaneously. This data is then stored in the minor loops until it is needed to be read out.

Bubbles move between major and minor loops through metal patterns called transfer gates that go back and forth between adjoining chevrons. Once a bubble in the major loop reaches a transfer gate, a current pulse to the gate sets up a localized magnetic field causing the bubble to migrate to a minor loop. By changing the pulse timing, a bubble can be transferred from a minor loop back to the major loop where it can be read out.

By manufacturing more minor loops on a chip than are required, a means of allowing for misshapen chevrons or other defects in the chip are provided. This redundancy allows defective minor loops to be circumvented in the final product. The locations of these loops are detected during memory testing and are recorded in a programmable read-only memory (ROM) or written into a minor loop of bubble memory called a boot loop.[3] During power up of the bubble memory card, the boot loop is read out and placed into random access memory (RAM) in the bubble memory controller. This ROM or RAM now contains a map of the defective loops in the bubble memory chip.

A string of data to be written into the bubble memory is normally entered one-bit-at-a-time into the major loop and shifted around the loop until the first data bit lines up with the first minor loop, the second bit aligns with the second minor loop, and so on. However, if some minor loops are defective, the locations to be written must be compared against the contents of the map memory. If the map memory signifies a defective loop, a "zero" is inserted in the data string so that no data ever enters a

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[3]"Bubble Memory Design Handbook", Intel Magnetics Inc. 1980

defective loop. At the other end, data being read out from the bubble memory must also be compared to the defective loop map in order that the bits in the output data string corresponding to bad loops can be stripped out of the string.[4]

The bubble memory housing contains the bubble memory chip, two permanent magnets, two mutually perpendicular coils and a magnetic shield which protects against external magnetic fields. The field of the two permanent magnets allows for the stable existence of the magnetic bubble domains and therefore the non-volatility of the system. The orthogonal coils provide a rotating magnetic field used to propagate the bubbles on the chip in a shift register fashion.

3. STATE OF BUBBLE MARKET

Rapidly declining prices for both semiconductor and magnetic-disk storage have made it difficult for magnetic bubble memory systems to compete as a cost-effective bulk storage system. With system density lower than that of floppy and hard disks, prices high and support hardware complex and difficult to apply, bubble memory manufacturers have had to focus their attention on specific advantages of the bubble memories. In applications where medium-speed, non-volatility, and tolerance of shock, vibration, and contaminants are needed, bubble memories are superior to disk systems.

To generate interest in bubbles as a mass storage device for microprocessor based equipment, manufacturers have come up with a variety of diversified packaging strategies with support hardware to ease interfacing. To promote the use of bubbles as a replacement for removable storage, devices such as floppy disk drives and tape cartridges, bubble makers have offered a new packaging tactic: the bubble cassette.[5] This new scheme adds removability to bubbles' other virtues and makes the system more flexible for those used to floppies while creating stiffer competition for non-removable Winchester disk drives.

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[4] Don Bryson, Dick Clover, and Dave Lee, "Megabit Bubble-Memory Chip Gets Support from LSI Family", Electronics, April 26, 1979, Page 105

[5] Steve Weitzner, "Bubble Cassettes Are on the Rise", Electronic Products, June 15, 1981, Page 41

Despite these efforts by bubble manufacturers to compete with other technologies, sales have not been as anticipated. The bubble memory technology has been difficult to master, and according to some industry analysts, the market was overestimated and the difficulty of entry was underestimated.[6] In the first three quarters of 1981 three manufacturers have stopped production of bubble memory chips and systems.

Rockwell was the first commercial manufacturer of bubble memory chips and support systems. Rockwell offered bubble memories up to 1 megabit per chip and bubble memory control boards. They were also the first to leave the commercial market in February, 1981.[7] Rockwell has said they will continue support of present customers and research into space qualified parts.

Texas Instruments withdrew from the bubble memory business in May of 1981.[8] They also stopped production of digital wristwatches and plasma displays which altogether lead to the layoff of 2,800 employees.[9] Texas Instruments had developed 92 K and 254 K bit devices for the commercial market which would have been more popular if they had had binary organized devices.[7] The company's later series of 256 K and 512 K and 1 megabit chips fixed this blunder, but the initial support chips for this new family had no error detection and correction capability. Texas Instruments had just introduced their bubble cassette system with the 512 K bit and the 1 megabit cartridge before pulling out of the market.

National Semiconductor had made bubble memory chips up to 256 K bits and was to introduce a 1 megabit device before it was reported on September 1, 1981 in Electronic Engineering Times that they had become the third U. S. manufacturer to stop production of bubble memory chips and systems. National cited poor sales as the reason for discontinuance. The company started its efforts three years ago, but sales had not even reached the $1 million mark.[6]

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[6]Warren Andrews, "The Bubble Bursts and National's Out", Electronic Engineering Times, Sept. 1, 1981, Page 1

[7]John G. Posa, "National Quits Bubble Market, Leaving Intel as Last U. S. Supplier", Electronics, Sept. 8, 1981, Page 41

[8]Jonah McLeod, "Bubble Memories Lose Leader as Texas Instruments Pulls Out", Electronic Design, June 25, 1981, Page 35

[9]Howard Wolff, "Will T.I.'s Defection Pop the Bubble?", Electronics, June 16, 1981, Page 93

Motorola plans to become a major manufacturer of bubble memories and is readying a new 11,000 square foot facility for fabricating bubble memory products.[9] Motorola had a second source agreement with National but does not view National's withdrawal as a setback.[6] Motorola's memories are now in the sampling stage and the company is planning production soon.[10] Motorola was also to produce support chips for National, but will now produce them only for themselves. It is not known if Motorola will produce a version of National's bubble cassette system, the "Bubleset", which offered a -20^{o} to $+70^{o}$ C operating temperature range.

Intel is the only major American bubble memory maker left. Intel feels that it will benefit by picking up the business left by the other three manufacturers.[6] They have reduced the price on volume orders of their systems and plan further significant price reductions in 1982. Intel Magnetics, which claims more than a 90% hold on U. S. sales, says the market for components alone excluding support circuits is $50 million and is expected to double in 1982.[7]

Intel offers the 7110 bubble memory chip, a 1 megabit device, incorporated into many different systems and subassemblies. The remainder of this report will focus on this device as the only one presently offered with the system level features required in the sounding rocket program.

4. INTEL MAGNETICS 7110

The Intel Magnetics 7110 is a serial-parallel-serial, shift-register magnetic bubble memory device with a binary page organization. Its storage elements are cylindrical bubble domains, 2.7 micrometers in diameter, occurring in a thin film of magnetic garnet material grown by liquid-phase epitaxy on a gadolinium-gallium-garnet wafer covering an area of 2 square centimeters.[4] After the film is grown, wafer processing is similar to that used with silicon. Standard photolithography practices are used to create the conductive and magnetic nickel-iron Permalloy patterns on the chip. The asymmetrical chevron patterns are used to form storage loops, input/output tracks, and the control elements.

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[10] Alex Mendelsohn, "Magnetic Bubbles Make Their Move", Electronic Products, May 1981, Page 25

The 7110 is a high density, 1 megabit, non-volatile magnetic bubble memory chip and housing. The gross capacity of the device is 1,310,720 bits of which 1,048,576 bits are usable for data storage.[11] The defect tolerant design incorporates major-minor loop architecture consisting of 320 storage loops, which allows for 64 redundant storage loops.[11] This excess storage provides for 48 defective loops to be bypassed, thus increasing chip yield and providing 16 extra storage loops to implement error correction.

To simplify system design, the 7110 is organized on a binary format as 256 data storage loops of 4096 bits each. The data is organized logically as a 512 bit page with a total of 2048 pages.[12] This allows the system to be configured as 128 K bytes of usable data storage.

In the serial-parallel-serial architecture, the 7110 has separate read and write tracks. The defective loop map is stored on-chip in a separate bootstrap loop along with an index address code. The boot loop is read out by the support electronics that in turn uses this information to mask out faulty loops in the main storage area.

The boot loop also contains a synchronization code that assigns page addresses to the data in the storage loops. Since the bubbles move from one storage location to the next on every field rotation, reference is made to the synchronization code and the number of field rotations that have elapsed in order to determine the actual physical location of a page of data. The same input and output tracks are used to write the boot loop as are used to access the main storage loops. The only difference is that the boot loop has independent swap (transfer) and replicate gates. The boot swap gate is only used at the factory to write the defective loop mask and synchronization codes. The boot replicate gate is accessed every time the memory chip and support electronics is powered up. During power up the support electronics reads and stores the mask information and synchronization codes to be used in operation. When power is disconnected, the 7110 retains the stored data.

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[11] "Magnetic Bubble Storage Data Catalog", Intel Corporation, Feb. 1981

[12] John Tsantes, "Far From Gone, Bubble Memories Thrive in Specialized Areas", EDN, Sept. 2, 1981, Page 53

The Intel 7110 bubble memory chip is organized as two identical 512 K bit half sections. Each of these half sections is divided into two 256 K bit sections referred to as quads.[3]

Each half section contains one boot loop attached to the major track of the even quad. Each quad consists of 80 identical 4096 bit storage loops, a bubble generator gate, input track, swap gates, replicating generator gates, output track, and a detector gate (Figure 3).

The generator operates by replicating a seed bubble that is always present at the generator site. The bubbles following generation are propagated down the input track. Bubbles are transferred back and forth between the input track and the storage loops by the swap (transfer) gates. These gates are spaced every four propagation cycles along the track. The swap gate is designed to function so that the space vacated by each bubble transferred out of each loop is filled by the bubble being transferred into each loop. The bubbles transferred out continue down the rest of the input track where they are destroyed by dumping them into a bubble bucket guard rail.

Bubbles need to be read out of the storage loops in a non-destructive fashion. This is accomplished by a set of replicate gates which are spaced every four propagation cycles along the output track. The replicate gate splits the bubble in two and places one bubble back in the storage loop while the other bubble is placed in the output track. The bubble in the output track propagates down the track to a detector that operates on the magneto-resistance principle. The detector consists of a chevron expander which enlarges the cylindrical bubble domain into a long strip domain. This strip domain is then transferred to the active portion of the detector which produces an output signal of a few millivolts. In the immediate vicinity of the detector is a "dummy" detector which produces a reference to be used by the external differential amplifier to cancel common mode pickup from the in-plane drive field.

The 7110 is packaged in a dual-in-line leadless package with permanent magnets, coils, and surrounding magnetic shield. The 20 pin leadless package requires a special socket manufactured by Molex Inc. (Figure 4).

COURTESY INTEL CORPORATION

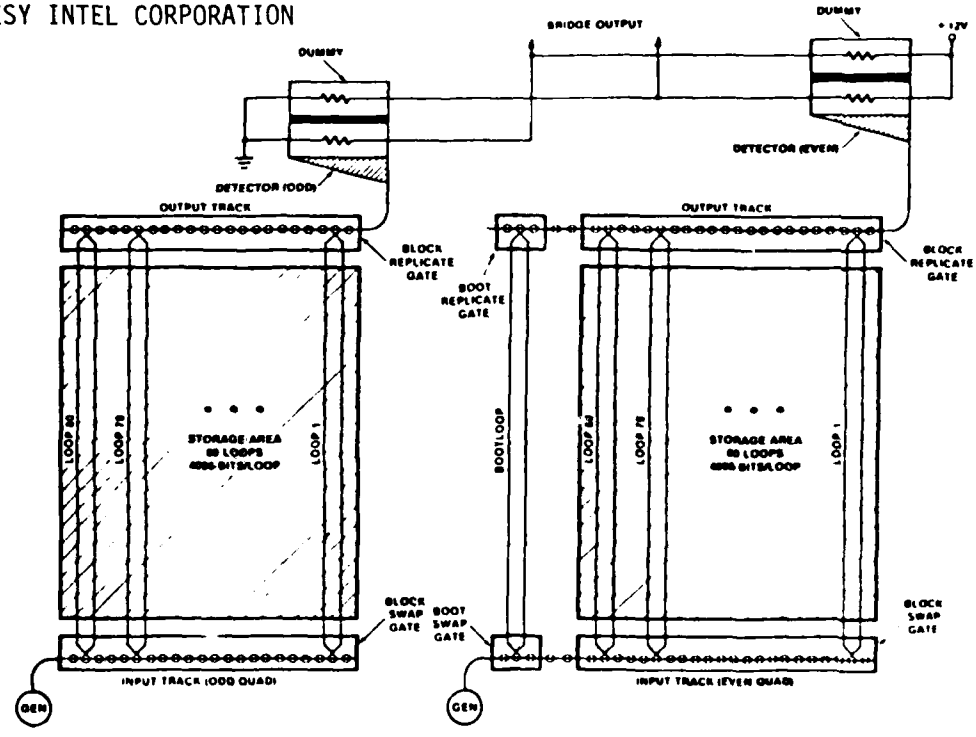

Figure 3. Major Track-Minor Loop Architecture of 7110 (One Half Shown)

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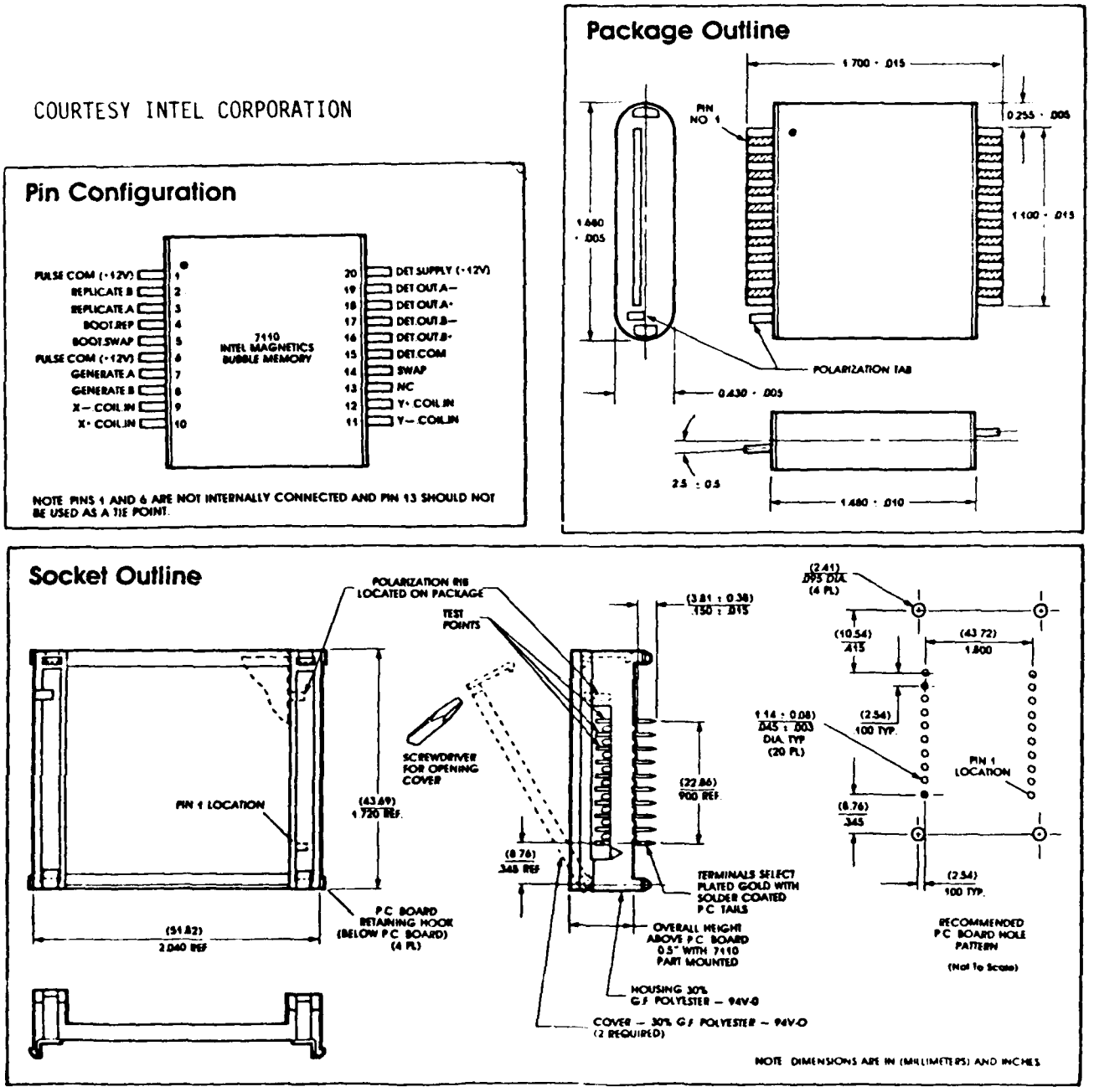

Figure 4. Package and Socket Outline

The permanent magnets produce a bias field to support the existence of the bubble domains. The package is constructed to maintain a 2.5 degree tilt between the plane of the bias magnet faces and the plane of the die.[3] This introduces a small component of the bias field into the plane of the die. When power is removed, this small in-plane field ensures that the bubbles will be confined to their appropriate storage locations. During operation when the drive coils are energized, this weak field component becomes negligible. The direction of the in-plane field is coincident with the 0^{o} phase direction of the drive field.[3]

Two orthogonal drive coils surround the bubble memory die. These coils, when excited by 90^{o} phase shifted triangular current waveforms, produce a rotating magnetic field in the plane of the die. This field is responsible for propagating the bubbles in the die. The shield serves to isolate the die from stray magnetic fields as well as providing a flux return path for the two permanent magnets.

The first part of a read operation replicates the bits of a page and places them on an output track to feed the detector bridge. The bits are shifted serially through the bridge so that the maximum data rate is twice the shift rate. During a write operation, the bits for a new page are first written serially on an input track. The bits are shifted until they coincide with the bits of the page they are to replace. A swap operation then exchanges the new page with the old at the address selected.

Knowing that the data rate is twice the shift rate, the performance of the 7110 can be estimated. Having a shift rate of 50 kilohertz, the maximum data rate becomes 100 kilohertz. With storage loops 4096 bits long, the average random access time of a page becomes about 40 milliseconds.[12]

To read or write a page of data requires a minimum of 327 shift cycles or 6.5 milliseconds. The average data rate is 78 kilohertz (512 bits per page divided by 6.5 ms).[4] This reduction from the maximum data rate is due to the overhead associated with the redundant storage loops.

5. 7110 SUPPORT COMPONENTS

To utilize the capabilities of bubble memories, the system designer must deal with an interface problem that is much more complex than that posed by

other memory technologies. The designer must provide for addressing and control logic for a sequential memory system, precise current pulse generation, low level analog voltage sensing, high current waveform generation, the ability to mask off bad loops, and error detection/correction.

An entire family of support parts is needed to ease this complex interface problem. Intel recognized this problem and offers four custom designed support chips (Figure 5). With this set of large scale integration (LSI) components, the system designer can focus on higher-level system objectives instead of learning the details of bubble memory interfacing.

The most important support chip for Intel's bubble memory system is the 7242 Dual Formatter/Sense Amplifier (FSA). The FSA is packaged in a standard 20 pin dual-in-line package and uses NMOS technology. The key functions of the 7242 are amplifying the low-level bubble signals, buffering data, handling redundant loops, and providing error detection and correction.

A standard microprocessor interface is provided by the Intel 7220 bubble memory controller (BMC). The controller is a 40 pin LSI device fabricated using HMOS technology. The first 7220 BMC had flaws in its design[13] and has been replaced by the 7220 BRD which is a board containing a 40 pin LSI chip surrounded by various smaller chips and components.[11] The 7220 BRD plugs into a 40 pin socket so that it can directly replace the 7220 BMC. The 7220 BRD provides an eight bit parallel interface, direct memory access (DMA) handshake capability, single or multiple page block transfers, and control for up to eight bubble storage systems.

Other support electronics handle the drive coils of the bubble memory. The currents needed for the coils are beyond the capacity of standard IC devices so a 7250 coil predriver (CPD) is used to interface between the 7220 and VMOS drive transistors (7254). The 7250 is a CMOS device in a 16 pin DIP. The Intel 7230 current pulse generator (CPG) is used to interface between the 7220 and the bubble memory device. It provides the fast, high current pulses required for the generate, swap, and replicate gates on the bubble memory chip. The 7230 is fabricated using Schottky bipolar technology and is housed in a 22 pin DIP.

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[13] Outlook, "Keeping the Fizz in Magnetic Bubbles", Electronic Products, August 1981, Page 17

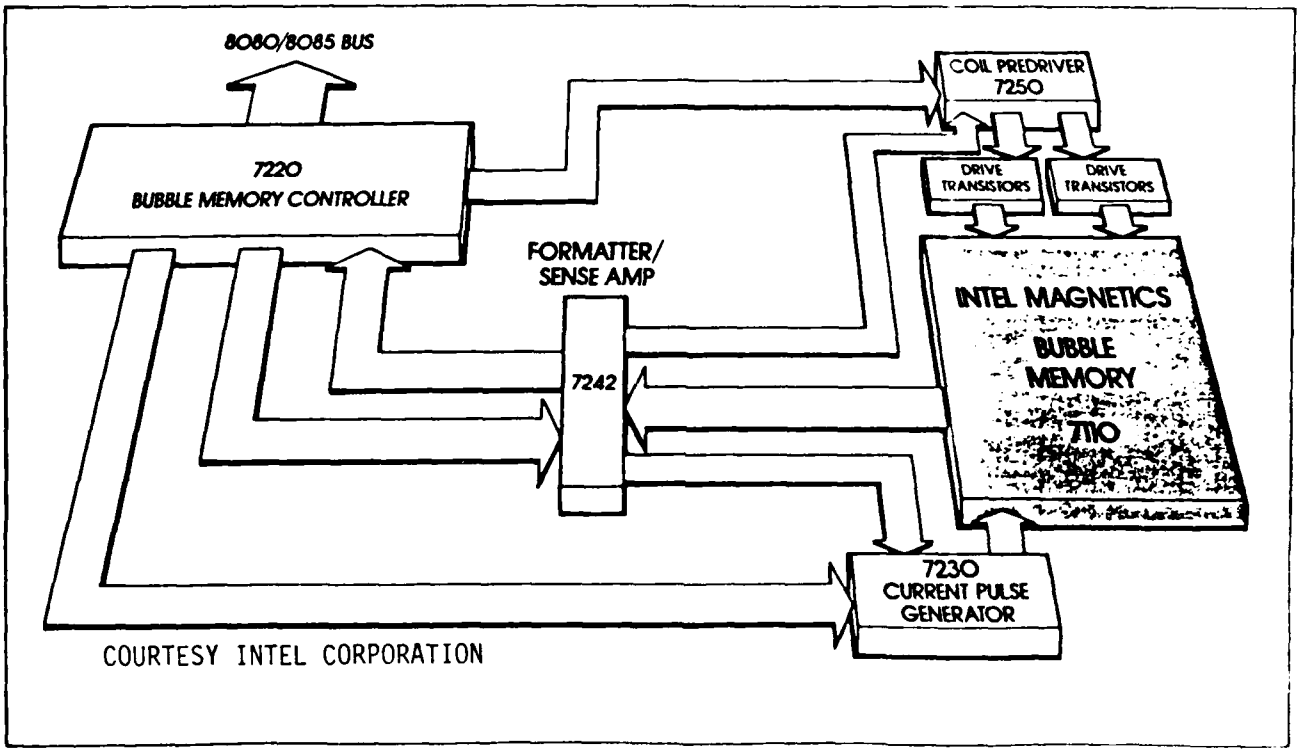


Figure 5. Block Diagram of Single Bubble Memory System -- 128K Bytes

Each channel of the 7242 FSA generates a 14 bit Fire code which it attaches to the end of each 256 bit data block when writing to the bubble memory. It uses this code to correct burst errors up to 5 bits long when the data is being read out. The 7220 BRD contains a 40 x 8 bit FIFO for buffering input and output data. The FIFO is capable of sustaining a 1 Megabyte/second transfer rate while room remains in the FIFO.[11]

With these basic components and a 7110, a minimum system of 128 kilobytes can be built on a 4" x 4" board (Figures 6, 7). The system operates from +12 and +5 volts only, with circuitry to monitor these voltages. If a power down occurs during a transfer, the controller will shut down the coil drivers in the proper sequence and preserve the integrity of the data, if power remains at acceptable levels for 100 microseconds.

The support chips are flexible enough to be used in varying system designs. In the first approach, provisions are made for paralleling controller chips. This provides for wider word widths in factors of eight bits (two controllers for 16 bit words). In the second scheme, one controller can control up to eight FSA's and, therefore, up to eight 7110s, one at a time. The 7220 has a chip select input and can, therefore, be multiplexed up to the limits of the host I/O.

The designer can also choose his method of transferring data on the system bus. The 7220 supports three methods of transfer: polled I/O, interrupt driven I/O, and direct memory access (DMA). The first two methods require the host processor be involved. The DMA mode allows data to be passed to host memory without host intervention.

Regardless of the method used, the host processor must initialize the system after powering up. This is accomplished by writing information relating to the desired operating modes into a set of addressable registers contained within the controller. After setting up the controller, the host issues an initialize command. This causes the controller to load the bootstrap loop register in the FSA with the defective loop mask and leaves the bubble device with page 0 ready to be read or written. The controller then issues an interrupt signaling it is ready for data transfers to begin. Read and write transfers may be specified from 1 to 2,048 pages. A seek command permits the user to predict his next read or write address, thus avoiding

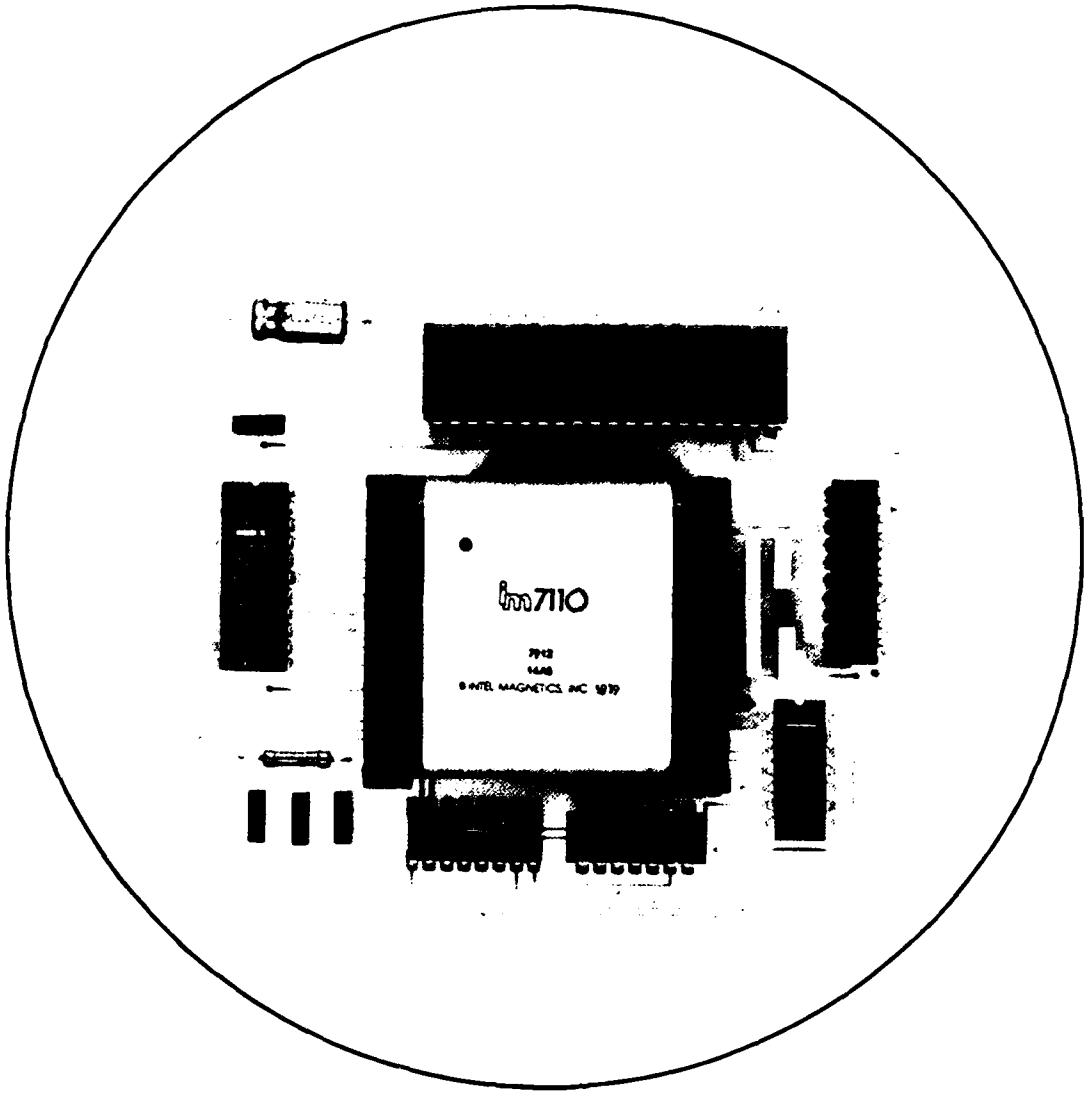
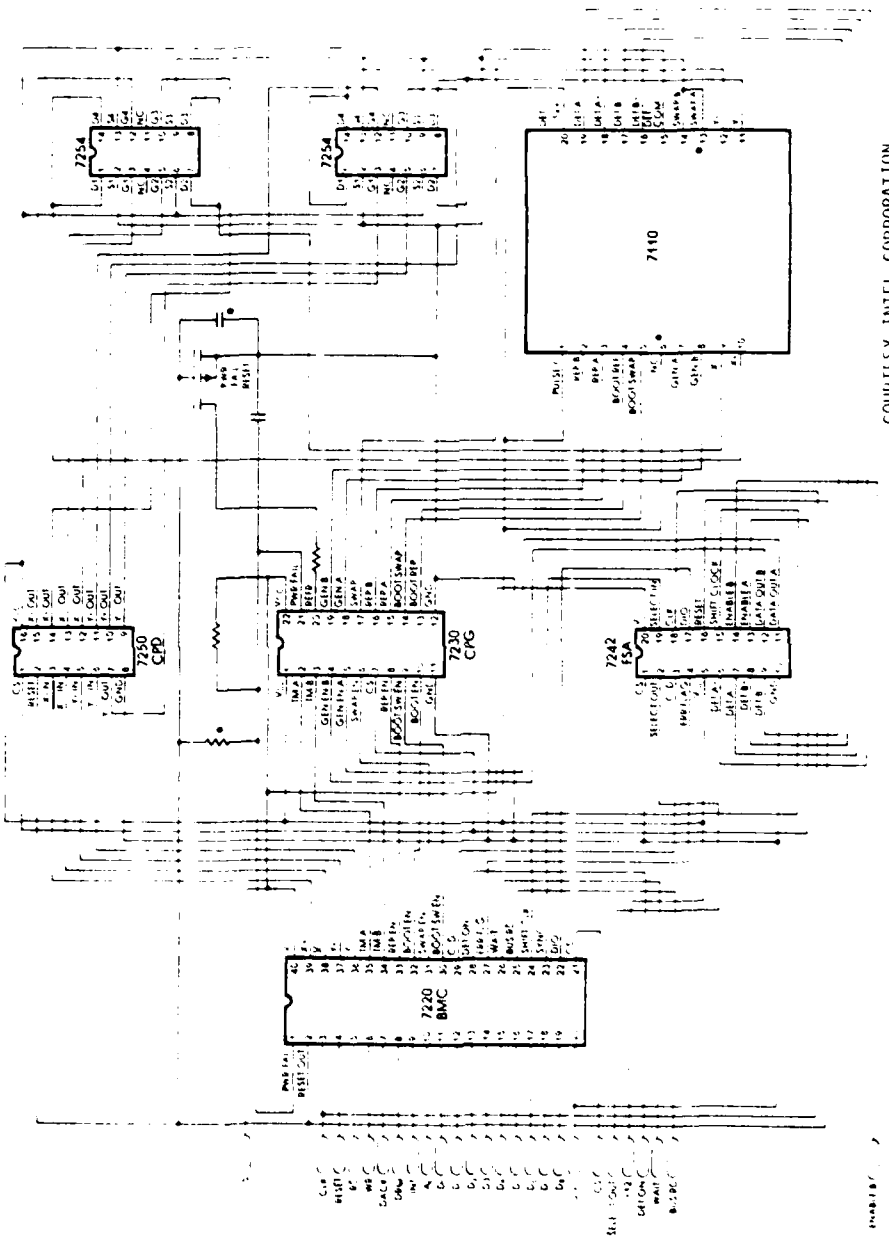


Figure 6. Complete One Megabit Bubble Memory System (shown actual size of 16 square inches) consists of 7110 bubble memory device and support electronics. (Courtesy Intel Corporation.)



COURTESY INTEL CORPORATION

Figure 7. System Interconnect Diagram

additional latency. Status bits are provided to the user and include a busy signal, a FIFO ready signal, a transfer complete flag, and several error flags. Status of the FSA may be determined with a special command. The interrupts can be masked to enable interrupts on errors, or just by operation complete interrupts.

6. INTEL PLUG-A-BUBBLE (iPAB)

The Plug-a-Bubble system is a bubble memory system designed for easy removal and replacement of the storage media similar to disc systems. In this case, the storage media is a sturdy aluminum casing housing a one megabit bubble memory. A basic system (iPAB-381) consists of a single iPAB-128 cassette and a single cassette holder.

The iPAB-128 cassette consists of a PC board, one 7110 MBM, all of the support components (including the 7220 controller), three LEDs, a number of discrete resistors and capacitors, and an aluminum casing that protects it from dust and shock. Intel's philosophy of putting all the support components in the cassette assures that they can be trimmed for each 7110, however, this makes the cassette large and very expensive.

The cassette holder provides a means of holding the cassette and a mating connector. The holder provides logic for the selection of the cassette, write protection logic, and bidirectional circuitry for gating and buffering of the data.

The iPAB system appears to be designed primarily for use with the iPAB-258 MMI/O card. This is an iSBX Multimode interface card available for users with processors that support the iSBX bus. If this card is not used, the user must generate the required signals for the cassette holder.

There are two modes that can be used to transfer data between the iPAB system and the host. They are the interrupt driven mode and the polled mode.[14] In the interrupt driven mode, an interrupt is issued whenever the 7220's FIFO becomes half full during a read or half empty during a write. In the polled mode, the host must periodically check the status register of the 7220 to determine whether service is needed. A direct memory access mode is possible, but requires some additional circuitry to accommodate handshaking.

[14]"Plug-A-Bubble Memory System", Intel Data sheet (Advance Information) 1981

7. THE STANDARD MEGABUBBLE

The Standard (STD) Megabubble is a self-contained, 1 megabit (Intel 7110) magnetic bubble memory system that fits on a single STD card. The card conforms to all STD bus specifications with the exception that the card is over the height specification and requires the space of two cards.

The STD Megabubble card provides extensive file-handling firmware resident in onboard PROM and is supported by RAM for internal buffering and control functions. The card is usable in interrupt driven, direct memory access, or polled system environments. It also features a full set of self-diagnostics and status indicators.

The user interface permits information to be stored and retrieved by file name rather than address location. This file-handling firmware isolates the user from the complex nature of the 7110 and provides open, close, read, write, delete, and insert file functions. The firmware also runs initialization, error checking, directory management, and internal diagnostics. Status indicators reveal memory full, bubble under access, fault, and write protection conditions.

The STD Megabubble card is designed for use in a microprocessor-based environment and requires one for full feature implementation. The card requires +5 volts at 1.5 amps maximum, and +12 volts at 40 milliamps maximum.[15] This translates to a power dissipation of about 8 watts. Two temperature versions of the 7110 are offered; one from 0-50° C, and the other 0-70° C.

8. 7110 RELIABILITY TESTS

The reliability of the 7110 is a function of the quality of design, the quality of parts, fabrication, the extent of the product testing, and feedback from testing. This section describes the reliability and environmental capabilities of the 7110.

Current densities in bubble memory devices are 10^6 to 10^7 amps/cm^2 but with duty factors of 1% or less. While extensive data exist for DC electromigration, less is known about electromigration under pulsed current conditions. The use of 4% Cu-Al conductors enhances electromigration lifetimes

[15] "STD Megabubble", Designsmiths Inc. data sheet

in the 7110. An extensive study was undertaken using increased temperature, current density, and duty factor as accelerating parameters. This study gives projected mean time to failure (MTTF) due to electromigration of the 7110 operating continuously at 70° C to be in excess of 100 years.[16]

The 7110 electrical joining consists of thermosonic bonding of 1.3 mil gold wire directly to the conductor level (AlCu) or detector pads (NiFe) of the chip. Aging at 200° C was used to determine if interdiffusion and chemical reaction would lead to premature bond lifting. Assuming a pan activation energy of 0.8eV for interactions between gold and AlCu or NiFe, then an aging time of 240 hours at 200° C is equivalent to 30 years at 70° C chip temperature.[16] All failures observed were wire breakage at the heel of the stitch bond, no cases of lifting of the pad were seen. This occurred using a minimum pull strength of 8 grams, which is well in excess of MIL-833B requirements of >4 grams.[17] Consequently, no long-term bonding problems should exist with the 7110 during its lifetime. Bond pull tests are performed on a routine monitor basis to ensure high quality process control.[18]

To determine moisture resistance of the 7110, steam tests were run without pin bias in a 15 PSI autoclave at 125° C. The tests were run on 10 parts with MTTF at about 96 hours. No failures have ever been observed at 48 hours.[18] Any change in line or coil resistance exceeding 1% also constituted a failure.

Relative humidity tests were conducted on 20 parts at 85° C and 85% humidity in three modes:

1) without pins biased
2) with pins biased but with no current flowing
3) with pins biased and detector dissipating power to induce a chip temperature rise.

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[16] "The 7110 One Megabit Magnetic Bubble Memory", Intel Magnetics Reliability Report RR22

[17] J. E. Davies, "Magnetic Bubble Reliability Testing--Component and System Level Aspects", IEEE Reliability Conf. (1980)

[18] J. E. Davies, "Reliability and Environmental Capabilities of the 7110, One-Megabit Bubble Memory", 1980 Wescon Professional Program

For all tests the MTTF exceeded 1000 hours, with no failures ever observed at 500 hours.[16]

Ten parts were subjected to a high temperature 150° C bake for 168 hours. No failures were observed and post bake operating margins remained unchanged.[16]

Temperature cycling of -65 to +150° C at 27 minutes per cycle was used to stress the mechanical integrity of the 7110. Of the 20 parts tested, 1 failed after 10 cycles with no further failures after 100 cycles.[16] Consequently, 10 cycles are used after final assembly as a 100% screen for infant mortality problems.

Shock and vibration tests were performed in both operating and non-operating modes. For the operating vibration mode, the system used was the minimum system on the 4" x 4" card with the 7110 installed in a socket. The mean failure point was 20Gs at 570 Hz, and the failure mode was breakage of the 7110 socket.[18] For the non-operating mode, ten parts were tested at 20Gs on 3 axes at 2Hz-20KHz sweep with no failures.[18] For shock testing, ten parts were tested at 200Gs on 3 axes with no failures.[18] For comparison, a graph is included showing the vibration amplitude and frequency data for the Black Brant and Aerobee class sounding rockets[19] (Figure 8).

Even though the Plug-A-Bubble Cassette System is basically a minimum subsystem with a small amount of interface hardware, it is only specified for 5Gs of vibration for the system.[14] Shock on 3 axes is specified as 40Gs for the cassette and 20Gs for the complete system.[14] It is not understood why this differs so much from the data on the minimum system unless the cassettes are not mounted very securely in the holder.

The 7110 is enclosed in a mumetal can to provide shielding of the chip from stray external magnetic fields. The worst case occurs when the external field opposes the bias field inside the package. Considering these worst case conditions, the package offers a minimum shielding of 20 oersteds with no measurable performance degradation.[18]

A number of simple tests were performed to simulate noisy electromagnetic environments. Systems which are immune to static discharge generally behave well in electromagnetic environments. This is because static

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[19] "Environmental Test Report ARC75 PCM Encoder", Lockheed Missiles and Space Company Inc.

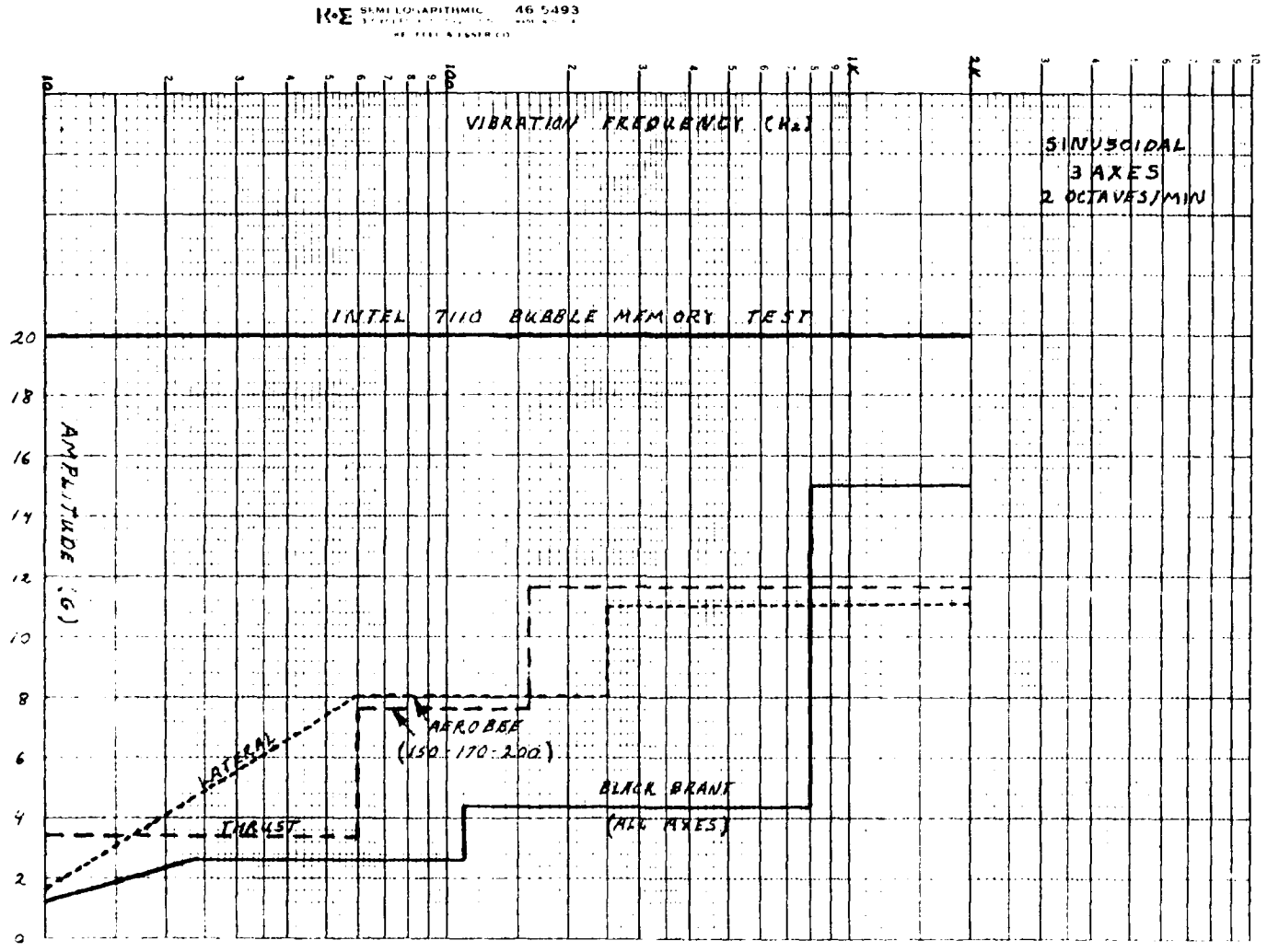

Figure 8. Vibration Data

discharge on a system chassis will radiate noise and induce noise in the wiring harnesses. Using the iSBX-250 board to exercise the 7110 and its support chip set in an Intellec II development system, a potential of 7 kilovolts was repeatedly discharged on the system chassis. No increase in error rate of the 7110 was observed.[18] Typical industrial noise sources such as a power drill, fluorescent light starter and printer motor power cable were operated ¼ inch from the 7110 and 7232 during error rate testing. Even operating close to the edges of the VDD and VCC voltage supply margins, no increase in errors was observed.[18]

The power level sense circuit built into the 7230 insures data integrity during a power fail or reduction in power levels by initiating a controlled system shutdown. The VDD and VCC supplies are each monitored separately and a low power level of either supply will trigger power fail. Since the 7230 is Schottky bipolar, the triggering of the power fail is fast. Assuming the worst case trigger is 11.1 volts for VDD and 4.5 volts for VCC and shutdown requires two field rotations or 42 microseconds, the 7110 is recommended to have a 100 micro farad filtering capacitor on both VDD and VCC to insure data integrity. The minimum power levels the system will see are 10.7 volts on VDD and 4.4 volts on VCC the instant before shut down is complete.[18] Characterization has shown these values to be safe.

These estimates were confirmed by removal of power from several iSBC-250 boards that were being error rate tested. Power to each board was removed several hundred times by turning off the Intellec II supply, pulling the power cord from the wall, and by pulling the board from its socket. Perfect data storage was obtained in all cases.[18] Furthermore, reseating the iSBC-250 in the chassis with power applied also had no affect on stored data.[18]

Although the widest operating range of the 7110 is 0^{o} C to 70^{o} C, data can be reliably stored over the full -65^{o} C to $+100^{o}$ C range. To confirm this, full megabit data patterns were written into twenty 7110 packages. Ten were stored at -40^{o} C and ten at $+50^{o}$ C. At weekly intervals the patterns were read and the parts interchanged from hot to cold and cold to hot storage. In excess of 50,000 device-hours of data storage was obtained without data loss.[18]

The primary design goal for the 7110 and its support chips was high system reliability. This was accomplished by the use of about 15% redundancy to allow for defective storage loops in the 7110. This not only improves yields, but, since the number of defective loops is nearly always less than the redundancy allows, weak loops can be bypassed, thus improving operating margins and data reliability. By the use of two bootloops on the 7110, each containing the address header code and defective loop map in triplicate, the 7220 controller can decide between bootloops in case of an error.

About a quarter million device hours have been accumulated on the 7110 and its support circuits at both nominal conditions and at the edges of temperature and voltage margins. The major error mode of the 7110 is the isolated single bit random error. On this type of error, error correction can operate extremely effectively. With error correction enabled, the effect on system level error rate is dramatic. At a 68KHz operating data rate and worst case operating conditions, the mean time between uncorrectable errors is in excess of 30 weeks.[18] With nominal supplies and at 25° C, the mean time between uncorrectable errors is greater than 1000 years, assuming errors are corrected by a rewrite and not left to accumulate.[18]

A one megabit subsystem requires one each of all support components and two 7254 drivers. Adding up the failure rate of all components except the 7110, one comes up with 0.34% per 1000 hours at 79° C.[20, 21] This translates into a MTTF of about 30 years. The MTTF of the one megabit system including the 7110 is about 0.6% per 1000 hours at 70° C continuous operation.[18] This translates into a MTTF in excess of 15 years for the complete subsystem at 70° C. Based upon the 250,000 device hours of life test data, the lifetime of the minimum subsystem is predicted to be in excess of 20 years for normal operation at 25° C.[18]

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[20] "HMOS Reliability", Intel Reliability Report RR18

[21] "N-Channel Enhancement Power MOSFET (VMOS)", Siliconix Inc. Reliability Report 2978

A 1 megabit system containing 64 packages of 16K EPROM would have a failure rate of 4% per 1000 hours[22] and a system of 16K dynamic RAM would have a failure rate of 1.1% per 1000 hours at 70° C.[23] Both of these calculations are based on the memory components alone. Additional failures would be expected to occur in the support circuits. It can be seen that the 0.6% failure rate of the 7110 and its support chips compares favorably with competing semiconductor technologies.

9. THE FUTURE BUBBLES

Unlike other bubble memory manufacturers, Intel claims business is too good to quit and plans development of a 4 megabit bubble memory chip and support circuits. Intel is presently shipping about 2000 units per month, which is three times more than last year.[11] Intel plans to boost production to about 8000 units per month in 1982.[11]

The 4 megabit chip is based on the same technology and design as the 1 megabit device. Intel already has the new controller chip breadboarded and has started characterizing some of the 4 megabit devices. All of the components for a minimum 4 megabit subsystem are expected for sampling in late 1982.[24]

Western Electric's Government Systems Division has begun developing a 2 megabit chip that is to operate under a -54 to +155° C range.[13] Under a contract awarded by the Department of Defense and NASA, the project is to develop new bubble technologies for use in military and space systems.

In Japan, Fujitsu and Hitachi both have plans to introduce 1 megabit devices and associated support chips. Fujitsu presently offers a 64 kilobit and a 256 kilobit bubble device in a bubble memory cassette.[12] Hitachi offers devices in 16K, 64K, and 256 kilobit chips with clock rates as high

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[22] "2716 16K UV Erasable PROM", Intel Reliability Report RR19

[23] "2116 N-Channel 16K Dynamic RAM", Intel Reliability Report RR16

[24] Dave Bursky, "Intel Pushes Ahead with it's 4-Megabit Bubble Memory", Electronic Design, Sept. 30, 1981, Page 31

as 500 kilohertz.[12] These smaller devices have limited use in the sounding rocket program, but the larger 1 megabit devices may have applications depending on their ruggedness. Hitachi reports research and development on a 4 megabit device while actively pursuing a goal of a 16 megabit device. The company plans to up the drive frequencies from 50 kilohertz to 500 kilohertz or 1 megahertz.[13]

A problem with scaling down Permalloy circuits to achieve higher densities and thus increase storage capacity, is that portions of the circuit pattern must have dimensions that are a fraction of the bubble's diameter. Therefore, structure features less than 1 micrometer are needed to control 1 micrometer diameter bubbles. These structures start to lie beyond current lithographic capabilities. This means the Permalloy technology used today may serve for 4 megabit devices but higher densities will require a departure from this architecture.

A new design, the contiguous disk, is being pursued at IBM and Bell Labs. In the contiguous disk technology, the bubbles move alongside the circuit pattern rather than under it. Lithographic features larger than the bubble diameter can be used, permitting storage densities of 4 megabit per square centimeter with 1 micrometer bubbles, or 16 megabit per square centimeter with .5 micrometer bubbles.[12] This technology also allows high bubble-propagation frequencies that are usually greater than 700 kilohertz.[12] Consequently, much higher operating speeds will be achievable.

10. APPLICATIONS IN ROCKETS

Easy application of bubble memories requires the use of the specially designed support chips. These support chips are primarily designed for use in or with a microprocessor-based system. Since the bubble memory controller requires a variety of commands in order to operate effectively, a microprocessor is almost a necessity for implementing a bubble memory system. The microprocessor, in turn, requires some amount of ROM to store a program and some RAM to use for stack pointers and scratch pad work.

Adding a microprocessor to the system would increase the power and space requirements unless it was also used for data compression or on-board data reduction. In either of these cases, fewer bubble memory chips would

be required to store the data and, consequently, less power and space would be required. The minimal 1 megabit subsystem operates off of +12 and +5 volts and consumes about 6 watts of power. Such a system with a microprocessor would draw about 10 watts.

A straightforward way of implementing a microprocessor-based memory system would be to use the STD bus system. This would allow the use of the wide variety of microprocessor and interface cards offered for the STD bus, as well as the STD Megabubble card. By having extra slots available in the card cage, multiple Megabubble cards could be added to increase the memory capacity needed for a particular mission. After the flight, the Megabubble cards could be removed and placed into another STD card cage at the data reduction sight where their contents would be read out by the host computer. One of the main advantages of the STD bus system is that the hardware can be completely implemented with off-the-shelf items. However, STD bus hardware would have to be ruggedized for use in sounding rockets. The Physical Science Laboratory is in the process of ruggedizing STD bus hardware for use on the space shuttle; this technique could be readily adapted to sounding rocket applications.

The Plug-A-Bubble system looks attractive because the aluminum cassettes are easily removed and are protected from damage even when removed from the system. However, the microprocessor and interface circuitry would have to be fabricated and memory expansion requires additional cassette holders. The vibration tolerance of the Plug-A-Bubble system is only 5Gs which may not be enough to insure reliable operation in sounding rockets.

A system using the 4" x 4" cards from the BPK-72 prototype kit can be built to allow expansion, but the microprocessor and interface circuits would still have to be designed for the system. These cards do not contain all the features found on the STD Megabubble card; however, they are less expensive and do have all the essential features needed for the sounding rocket program.

The Intel 7110 and its associated support chips are rugged enough to withstand the vibration in sounding rockets, provided they are securely mounted in the chassis. Though the 7110 and its support chips are only

offered in commercial temperature ranges, temperatures in sounding rockets seldom deviate outside of this range. Electronics used in previous flights have consisted of commercial temperature chips and have survived numerous flights. Therefore, a bubble system should be expected to survive repeated flights in sounding rockets.

Even though a megabit of data storage is a lot of storage capacity, in a data collection environment it can quickly be expended. Using a single 1 megabit bubble memory chip and storing ten bit data words at the maximum word rate of 10 kilohertz, the memory capacity would be reached in about 10 seconds. Using the same system to replace one channel on a PCM encoder would slow the word rate down to 625 samples per second. At this rate, memory capacity would be reached in 167 seconds, allowing data to be collected for 2.8 minutes. A 4 megabit chip would enable data at the 625 samples per second rate to be collected for 11.2 minutes, a more reasonable time for a sounding rocket flight.

11. COMPARISON OF BUBBLE MEMORY WITH A DIGITAL TAPE RECORDER

A comparison between bubble memories and a digital tape recorder system for sounding rocket applications is in order. The SETS-1 Severe Environment Digital Tape System, which is a 23 megabit digital recorder designed for use in severe environments, has been chosen to make this comparison. The SETS-1 is hermetically sealed in a compact, ruggedized package. It consists of a drive module and a removable tape module that together measures 4 x 4 x 6 inches and weighs 4.5 lbs. The recorder has four tracks, each capable of storing 48,000 bits per second. The tape speed is 30 inches per second (ips) for read or write functions and 120 ips for search or rewind. The tape module contains 300 feet of tape, providing 120 seconds of recording time. The unit is capable of operating over a temperature range of -40° C to 70° C, in 0-100% condensating humidity, and to an altitude of 70,000 feet. Power consumption is 25 watts, and the recorder unit is conduction cooled.[26]

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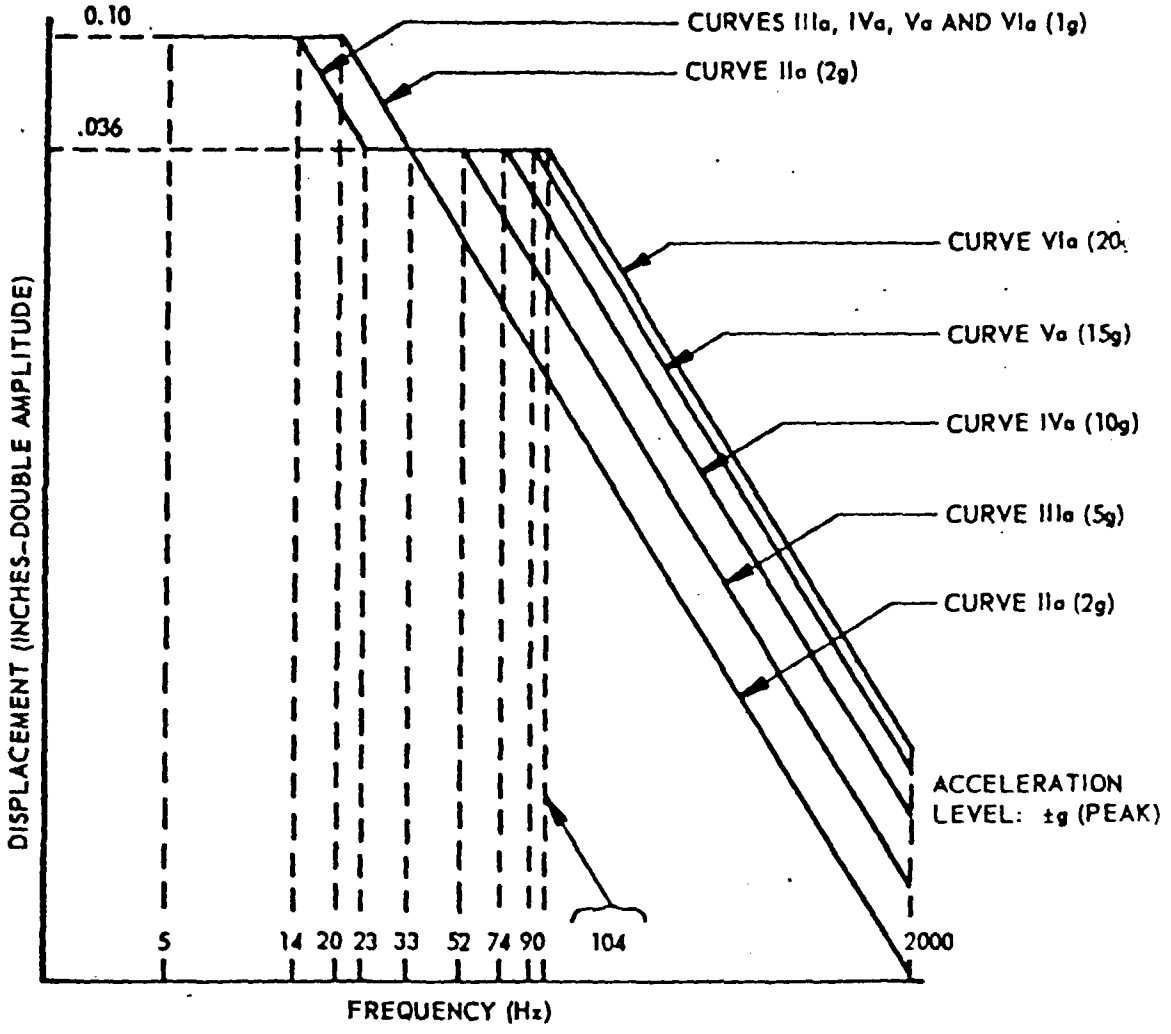
[26] "SETS-1: Severe Environment Digital Tape System Data Sheet", Severe Environment Systems Company; Chatsworth, CA

Other features of the SETS-1 include the following: (1) auto stop at either the beginning or end of tape; (2) 60 millisecond start/stop time; and (3) TTL compatible control commands. Control commands and/or status indications include: data in/data out, run/stop, slow/fast, forward/reverse, strobe, enable, sense level, output enable, data reset, running, at speed, tack pulses, file protect, end of tape, beginning of tape, drive ready and tape ready. The SETS-1 meets MIL-E-5400, MIL-E-16400 and MIL-E-4158 for equipment; MIL-Q-9858A for quality; and MIL-STD-883, Level B for microcircuits. The drive module costs $8,800 and the tape modules are $1,750 each.[26]

A comparison between the SETS-1 Tape Recorder and the Intel 7110 Bubble Memory will show that the tape system can store 23 times as much data as a single bubble memory chip is capable of storing. Bubble memory storage capacity, however, can be expanded within the limitations imposed by power consumption and size constraints. The tape system can acquire data nearly twice as fast as a single bubble memory unit. Unfortunately, though, if the data rate is slower than 48,000 bits per second, then some of the tape recorder's storage capacity will be wasted because the tape runs at a fixed speed of 30 ips. Furthermore, any formatting required for storing the data on tape will also reduce the available data storage capacity. If the data to be stored occurs in intermittent bursts, the tape recorder can be started and stopped several times over a several minute period to record a maximum of two minutes worth of data. This technique may be satisfactory for some sounding rocket applications. The altitude limitation of 70,000 feet means the SETS-1 would not be usable unless placed in a pressurized compartment, whereas the Intel 7110 can be used in space. And, although the power consumption of the SETS-1 is higher than a single Intel 7110, it is considerably less than that required for 23 of the Intel 7110s. Therefore, specific system requirements must be known in order to adequately compare power consumption between the two approaches.

A primary advantage of bubble memories over digital tape recorders for sounding rocket applications is their tolerance of vibration. The SETS-1 system is specified to handle 5 Gs of vibration (Curve IIIa in Figure 9),[26] whereas the Intel 7110 is specified for 20 Gs (Curve VIa). Since small sounding rockets undergo vibration in excess of 5 Gs (see Figure 8), the SETS-1 will require vibration isolation in order to be used in sounding rockets.



CURVE Ia (OF PREVIOUS ISSUES) – REPLACED BY CURVE IVa
CURVE IIa – EQUIPMENT DESIGNED FOR OPERATION ON ISOLATORS WITH ISOLATORS REMOVED
CURVE IIIa – EQUIPMENT MOUNTED IN FORWARD HALF OF FUSELAGE OR IN WING AREA WITH ENGINES AT REAR OF FUSELAGE
CURVE IVa – EQUIPMENT MOUNTED IN REAR HALF OF FUSELAGE OR IN WING AREA WITH WING OR FRONT MOUNTED ENGINES
CURVE Va – EQUIPMENT MOUNTED IN ENGINE COMPARTMENT OR ENGINE PYLON
CURVE VIa – EQUIPMENT MOUNTED DIRECTLY ON ENGINE

Figure 9. Sinusoidal vibration requirements for equipment designed for installation in jet airplanes (Taken from MIL-E-5400T, 16 Nov. 1979, Page 31)

In summary, the main advantage of the digital tape recorder over bubble memories, on a one-for-one basis, is the amount and rate of data storage capability. Bubble memories, on the other hand, have a much higher vibration tolerance and are much more compatible with the physical environment of sounding rockets than are digital tape recorders.

12. CONCLUSION

With increases in accumulated data and the consequent crowding of the RF spectrum, bubble memories are an attractive media for on-board mass storage systems in sounding rockets. Bubble memories have been shown to be highly reliable devices both in terms of data integrity and freedom from failure. Their tolerance of shock and vibration show bubble memories to be rugged enough to survive the harsh environment offered by sounding rockets. Ruggedness and compatibility with the environment of sounding rockets are distinct advantages of bubble memories over a currently available digital tape recorder that could be adapted for use in sounding rockets; however, the tape recorder has a significant advantage in storage capacity over presently available bubble memories. Presently available bubble memories can store up to 1 megabit of data. Future bubble memories promise to be even larger in storage capacity and lower in price per bit. Magnetic bubble memories have proven to be extremely rugged, large storage capacity devices that have the potential for certain specific applications in the AFGL sounding rocket program. For some future mission, for example, it may be desirable to provide on board, non-volatile storage of a few mission critical parameters for post mission evaluation as an assurance against permanent loss of these parameters in case of failure in the primary transmission or recording medium. Another potential application of bubble memories in sounding rockets would be for the acquisition of one or several short bursts of data, or for the storage of data only during the occurrence of specific events when a telemetry channel is either unavailable or it is undesirable to obligate one full telemetry channel to this data. Data storage can be initiated by remote commands, on board timing signals, or by a conditioned signal from the event itself. With the addition of limited intelligence, on board decisions can be made to select, prioritize and initiate data storage in a bubble memory.

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24. Dave Bursky, "Intel Pushes Ahead with it's 4-Megabit Bubble Memory", Electronic Design, Sept. 30, 1981, Page 31

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26. "SETS-1: Severe Environment Digital Tape System Data Sheet", Severe Environment Systems Company; Chatsworth, CA

LIST OF ABBREVIATIONS

BMC	Bubble Memory Controller
BRD	Board (Circuit)
CMOS	Complimentary Symmetry Metal Oxide Semiconductor
CPD	Coil Predriver
CPG	Current Pulse Generator
DC	Direct Current
DIP	Dual In-line Package
DMA	Direct Memory Access
EPROM	Erasable Programmable Read Only Memory
FIFO	First In First Out
FSA	Formatter/Sense Amplifier
HMOS	H-Type Metal Oxide Semiconductor
HZ	Hertz (Cycles per Second)
iPAB	Manufacturer's Designation (Intel Plug-a-Bubble)
iSBC	Manufacturer's Designation (Intel Single Board Computer)
iSBX	Manufacturer's Designation (Intel Single Board Miscellaneous)
IC	Integrated Circuit
I/O	Input/Output
K	Kilo
KHz	Kilohertz
LED	Light Emitting Diode
LSI	Large Scale Integration
MBM	Magnetic Bubble Memory
MTTF	Mean Time to Failure
NMOS	N-Type Metal Oxide Semiconductor
PCM	Pulse Code Modulation
PROM	Programmable Read Only Memory
PSI	Pounds per Square Inch
RAM	Random Access Memory
ROM	Read Only Memory
RF	Radio Frequency
STD	Standard

LIST OF ABBREVIATIONS (Cont'd)

VCC, VDD	Power Supply Voltage Designations
VMOS	V-Type Metal Oxide Semiconductor

APPENDIX A BUBBLE MEMORY PRICES[25]

INTEL MAGNETICS, INC.

July 6, 1981

BPK70	One Megabit Bubble Memory Subsystem Containing: 7110 MBM, 7230 CPG, 7242 FSA, 7250 CPD, 7254 Drivers (Prices shown are for quantities of 1-9)	
BPK70	S9014 Temp. Range = -20° C to $+85^{\circ}$ C	$3,145.00
BPK70-0	Temp. Range = 0° C to $+50^{\circ}$ C	1,815.00
BPK70-1	Temp. Range = 0° C to $+70^{\circ}$ C	2,015.00
BPK70-2	Temp. Range = $+10^{\circ}$ C to $+50^{\circ}$ C	1,615.00
BPK72	Bubble memory prototype kit for a minimal One Megabit System including documentation, IMB-72 blank printed circuit card, and: 7110 MBM, 7220 BRD, 7230 CPG, 7242 FSA, 7250 CPD, 7254 Drivers (Prices shown are for quantities of 1-9)	
BPK72	S9014 Temp. Range = -20° C to $+85^{\circ}$ C	$3,495.00
BPK72-0	Temp. Range = 0° C to 50° C	1,995.00
BPK72-1	Temp. Range = 0° C to 70° C	2,195.00
BPK72-2	Temp. Range = 10° C to 50° C	1,795.00
SBC 254-1A	128K Byte Multibus Bubble Board for OEM systems. Bubble memory boards with Multibus Interface. Contains one 7110 MBM, 7220 controller, 8257 DMA controller and support circuitry	$3,500.00
SBC 254-2A	256K Byte Multibus Bubble Board for OEM systems. Same as above but contains two 7110 MBM and support	5,600.00
SBC 254-4A	512K Byte Multibus Bubble Board for OEM systems. Same as above but contains four 7110 MBM and support	9,650.00

[25]"Intel OEM Price List", Intel Corporation, July 6, 1981

RUGGEDIZED PLUG-A-BUBBLE SYSTEMS

iPAB-381	The basic Plug-A-Bubble system consisting of one iPAB-128 cassette and one cassette holder. The iPAB-128 contains one 7110 MBM for 128K Bytes of storage, a 7220 controller and support circuitry. The cassette holder mates to the cassette via a connector and provides logic for cassette selection and write protect logic. The cassette holder dimensions are 7.75" x 3.8" x 1". Ambient operating temperature range = 0^{o} C to $+55^{o}$ C.	$3,490.00
iPAB-128	Optional extra Plug-A-Bubble system 118K Byte cassettes housed in cast aluminum and designed to withstand 40Gs shock on 3 axes. Dimensions are 6.1" x 3.6" x .81". When fully inserted in the holder, the cassette extends 2.5" from the end of the holder. Ambient operating temperature range = 0^{o} C to $+55^{o}$ C; non operating range = 40^{o} C to $+100^{o}$ C.	$3,150.00
iPAB-525	The optional iPAB-525 is a 5.75" x 3.25" x 8" chassis housing two iPAG-381 cassette holders. It occupies the same space as a 5.25" disc drive.	$1,080.00
iPAB-0362	Optional 36" shielded cable with connectors for two cassette holders. Typically this cabling will be used by OEMs who are designing their own interface card for connection to the Plug-A-Bubble system.	$ 130.00

DESIGNSMITHS, INC.[15]

STD MEGABUBBLE STD bus compatible bubble memory card containing one 7110 MBM, 7220 controller, file handling firmware, and support circuits. Ambient operating temperature 0^{o} C to 50^{o} C.	$3,550.00
Ambient operating temperature 0^{o} C to 70^{o} C.	$3,800.00


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